REMARKS

Claims 1-4, 6-23 and 26-28 are pending in this application. By this Amendment, claim 25 is cancelled without prejudice to or disclaimer of the subject matter contained therein, and claims 19 and 20 are amended to recite features supported in the specification on page 18, lines 13-19. No new matter is added by any of these amendments.

Applicants appreciate the courtesies extended to Applicants' representative by Examiner Ferris during the November 3, 2003 telephone interview.

Applicants gratefully acknowledge that the Office Action indicates that claims 1-4 and 6-18 are allowed. However, Applicants assert that claims 19-23 and 26-28 are also allowable for the reasons discussed below.

Reconsideration based on the following remarks is respectfully requested.

I. Request for Acknowledgement that References are Considered of Record

An Information Disclosure Statement with Form PTO-1449 was filed on March 31, 2004. Applicants have not yet received back from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the cited disclosed information. The Examiner is requested to initial and return to the undersigned a copy of the subject Form PTO-1449. For the convenience of the Examiner, a copy of that form is attached.

II. Claim 19 Satisfies the Requirements under 35 U.S.C. §112, second paragraph

The Office Action rejects claim 19 under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 19 has been amended to obviate this rejection in view of the Examiner's helpful comments. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

III. Claims 19 and 20 Define Over the Applied Reference

The Office Action rejects claims 19 and 20 under 35 U.S.C. §102(b) over U.S. Patent 6,240,377 to Kai *et al.* (Kai). This rejection is respectfully traversed.

Kai has an issue date of May 29, 2001. Applicants' filing date is March 21, 2000 and thereby antecedes Kai. Thus, Applicants respectfully submit that Kai is not a proper reference under 35 U.S.C. §102(b).

Also, a claim must be anticipated for a proper rejection under §102(a), (b) and (e). This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." See MPEP §2131. Even if the basis of rejection under §102(b) over Kai is replaced by §102(e), Applicants submit that Kai fails to disclose all the features recited in Applicants' claims.

Kai does not teach or suggest an emulation method including, *inter alia*, sending external signals for an external bus being connectable to an emulation memory and an external memory other than the emulation memory, the external terminals being connected to at least the emulation memory through the external bus when the microcomputer is in an emulation mode and being connected to the external memory without being connected to the emulation memory when the microcomputer is not in the emulation mode, connecting a bus of the processor to the external bus by a bus controller so that an access of the processor to an internal memory will be switched to an access to the emulation memory through the external bus when the microcomputer is in the emulation mode, outputting first and second control signals by a memory controller for controlling the external memory and the emulation memory, respectively, the second control signal being different from the first control signal and includes a memory read signal, as recited in claim 19.

Further Kai fails to teach or suggest a microcomputer including, *inter alia*, a memory controller which is connectable to the emulation memory and the external memory, and outputs a first control signal for controlling the external memory and a second control signal for controlling the emulation memory, the second control signal being different from the first control signal and including a memory read signal, wherein said second control signal includes a second memory read signal which becomes active at a timing earlier than that of a

first memory read signal included in said first control signal, as recited in claim 20. Thus, the rejected independent claims are patentable over Kai.

Instead, Kai discloses an emulator 30 with an emulation chip 31. In particular, Kai teaches the emulator 30 as including an emulation memory 37 and an emulation circuit 38. Kai further teaches the emulation chip 31 as having an EEPROM 34, a CPU 33 and an EEPROM controller 40 connected to the CPU 33 via a memory interconnect bus 39. A peripheral circuit interconnect bus 36 connects the EEPROM controller 40, the CPU 33 and a peripheral circuit 35. The EEPROM 34 connects to the EEPROM controller 40 via an interconnect bus 45. The EEPROM controller 40 accesses the EEPROM 34 via the peripheral circuit interconnect bus 36 during emulation or the memory interconnect bus 39 during normal operation. See col. 3, line 38 – col. 4, lines 37, 62-66 and Fig. 1 of Kai.

An exemplary embodiment of Applicants' features recited in claim 20 is shown in Figs. 2 and 4. In particular, a memory control unit (20) outputs a second control signal CNT2 (that includes RD2 in Fig. 4) which differs from a first control signal CNT1 (that includes RD1 in Fig. 4). As shown in Fig. 4, timing events B15 and B18 represent the activation timing for the first and second memory read signals RD1 and RD2, respectively. The timing B18 occurs earlier than the timing B15, so that the second memory read signal is activated earlier than the first memory read signal.

Further, as shown in Fig. 4, when timing B18 is delayed to the extent of timing B15, the processor fails to fetch an instruction from the emulation memory. Therefore, the claimed features inhibit executing instructions for instruction fetching and instructing decoding when a microprocessor on evaluation is operated with a clock frequency as high as operating a microcomputer on production, as shown in Fig. 4.

On the other hand, when timing B15 is shifted as early as B18, the external memory, such as EEPROM, cannot latch the address from the microcomputer. In other words, the external memory latches the address from the microcomputer, shown by a readout period B10

at timing B15, when the memory read signal RD1 becomes active. Nevertheless, when timing B15 is shifted as early as timing B18, the external memory (which operates slowly) fails to latch the address.

As recited in Applicants' claimed features, the memory read signals RD1 and RD2 (for the first and second control signals, respectively) differ from each other. Therefore, the features in claim 20 enable signal control which may set the RD1 signal active at an early timing, shown by timing B18, upon reading out of an instruction from the emulation memory, and set the RD2 signal active at a later timing, shown by timing B15 upon reading out information from the external memory. Consequently, it is possible to operate a microcomputer on evaluation with a clock frequency as high as operating a microcomputer on production, and effectively prevent failure to read-out an instruction from the emulation memory and information memory from the external memory.

Kai lacks an external memory other than the emulation memory and a memory controller for connecting a first access between an internal memory and to either the emulation memory or else the external memory, as recited in the claims. Further, Kai lacks features for providing the advantages as provided in Applicants' recited features, particularly for claim 20. Thus, Kai fails to anticipate Applicants' claimed subject matter. Withdrawal of the §102 rejection is respectfully requested.

IV. Claims 19-23 and 26-28 Define Patentable Subject Matter

The Office Action further rejects claims 19 and 20 under 35 U.S.C. §103(a) over U.S. Patent 5,313,618 to Pawloski *et al.* (Pawloski '618) in view of U.S. Patent 5,623,673 to Gephardt *et al.* (Gephardt). This rejection is rendered moot with respect to claim 25 and respectfully traversed for the remaining cliams.

A *prima facie* case of obviousness for a §103 rejection requires satisfaction of three basic criteria: there must be some suggestion or motivation either in the references or knowledge generally available to modify the references or combine reference teachings, a

reasonable expectation of success, and the references must teach or suggest all the claim limitations. See MPEP §706.02(j). Applicants respectfully assert that the Office Action has not satisfied this burden with the applied references regarding Applicants' claimed features, including the advantages as explained *supra* regarding claim 20.

Also, Pawloski '618 and Gephardt do not teach or suggest an emulation method including, *inter alia*, sending external signals for an external bus being connectable to an emulation memory and an external memory other than the emulation memory, connecting a bus of the processor to the external bus by a bus controller so that an access of the processor to an internal memory will be switched to an access to the emulation memory through the external bus when the microcomputer is in the emulation mode, outputting first and second control signals by a memory controller for controlling the external memory and the emulation memory, respectively, the second control signal being different from the first control signal and including a memory read signal, as recited in claim 19.

Nor do Pawloski '618 and Gephardt teach or suggest a microcomputer including, *inter alia*, a memory controller connectable to the emulation memory and the external memory, and outputs a first control signal for controlling the external memory and a second control signal for controlling the emulation memory, the second control signal being different from the first control signal, and including a memory read signal, wherein said second control signal includes a second memory read signal which becomes active at a timing earlier than that of a first memory read signal included in said first control signal, as recited in claim 20.

Instead, Pawloski '618 discloses an emulator system with shared emulator memory. In particular, Pawloski '618 teaches an emulation memory 206 connected to a controller 202 and an emulation microcontroller 204. The emulation memory 206 is connected to the controllers 202, 204 via address and data busses 208, 210, and is accessed via an address latch 212 and a multiplexer 220. Pawloski '618 lacks any teaching for a control signal including a memory read signal, as provided in Applicants' claims.

Pawloski '618 teaches that the controller 202 also accesses firmware memory 262 via an address latch 260. See col. 9, lines 13-30, col. 9, line 64 – col. 10, line 6, col. 10, lines 25-42, col. 10, lines 62-67 and Fig. 2 of Pawloski '618. By providing two processors, both accessing a single emulation memory instead of a processor accessing separate external and emulation memories, Pawloski '618 teaches away from Applicants' claimed features.

Gephardt does not compensate for the deficiencies of Pawloski '618 outlined above for claims 1, 19 and 20. Instead, Gephardt discloses an emulation memory mapping and locking method. In particular, Gephardt teaches a computer system 200 having a processor core 202 coupled to an interrupt control unit 204 and a memory control 208 that connects to a system memory 210. The memory control unit 208 includes a data buffer 212, address control 214 and a lock-out register 216. When the processor core 202 accesses normal memory space, the memory control unit 208 translates to system memory addresses. The interrupt control unit 204 transitions the state of the processor core 202 to "debug" mode, and reads the value of an ICE vector. See col. 4, lines 25-33, col. 5, lines 61-66, col. 8, lines 31-41 and Fig. 2 of Gephardt.

Further, there is no motivation to combine features related to the dual-processor emulator of Pawloski '618 with the mapping and lock-out method of Gephardt, nor has the Office Action established sufficient motivation or a *prima facie* case of obviousness. Even assuming that motivation to combine the applied references is established, the combination fails to teach or suggest Applicants' claimed features for either of claims 19 and 20.

The Office Action further rejects claims 21-23 and 25-28 under 35 U.S.C. §103(a) over 4,939,637 to Pawloski (Pawloski '637) in view of Gephardt. This rejection is respectfully traversed.

Claims 21-23 and 26-28 depend from claim 20. Applicants assert that at minimum the Office Action would be expected to apply Pawloski '618 and Gephardt under §103(a), as applied with claim 20.

However, the Office Action instead applies Pawloski '637 and Gephardt. The Office Action provides no explanation as to how Pawloski '637 provides for all the features recited in claim 20, while compensating for features recited in claims 21-23 and 26-28.

Pawloski '637 also does not compensate for the deficiencies of Gephardt outlined above for claims 19 and 20. Nor does Pawloski '637 teach, disclose or suggest the additional features recited in claims 21-23 and 26-28. Instead, Pawloski '637 discloses a circuitry for an emulation mode.

In particular, Pawloski '637 teaches a processor 100 connected to data bus lines 101 and address bus lines 102, with emulation mode input from a block 124 to AND gates 129 and 130 via conductor 128. The block 124 includes a D-type latch 142 to produce a circuit for generating an "emulator mode" signal at the Q output. See col. 9, line 19 – col. 10, line 45 and Figs. 5 and 6 of Pawloski '637.

Further, there is no motivation to combine features related to the emulator mode signal generating circuit of Pawloski '637 with the memory mapping and lock-out method of Gephardt, nor has the Office Action established sufficient motivation or a *prima facie* case of obviousness. Even assuming that motivation to combine the applied references is established, the combination fails to teach or suggest Applicants' recited features for claims 21-23 and 26-28.

For at least these reasons, Applicants respectfully assert that the rejected independent claims are now patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite.

Consequently, all the claims are in condition for allowance. Thus, Applicants respectfully request that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

V. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:GWT/gwt

Attachment:
Copy of earlier filed PTO-1449

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